

IN THE CLAIMS

1. (currently amended): A semiconductor device comprising:
an N type polysilicon gate and a P type polysilicon gate, ~~[[s]]~~ both disposed simultaneously, together occupying a first total area; and
~~wherein a dummy gate made of non-doped polysilicon for polysilicon gate etching is~~
disposed ~~[[in]]~~ contiguous to at least one of the N type polysilicon gate and the P type polysilicon gate, the non-doped polysilicon occupying a second area larger than the first total area of the N type and P type polysilicon gates.

2. (currently amended): The semiconductor device according to claim 1, wherein impurities for the N type polysilicon gate and the P type polysilicon gate ~~[[are]]~~ comprise phosphor and boron respectively.

3. (currently amended): A dry etching method for a semiconductor device, comprising the following steps of:

simultaneously gate-etching an N type polysilicon gate and a P type polysilicon gate; and
setting an etching area ~~of a dummy gate made of~~ occupied by non-doped polysilicon, ~~for polysilicon gate etching~~ which is contiguous to at least one of the N type polysilicon gate and the P type polysilicon gate, larger than ~~[[the]]~~ a total area of the N type polysilicon gate and the P type polysilicon gate, ~~to carry out said gate etching.~~

4. (currently amended): The dry etching method according to claim 3, wherein said gate etching ~~[[is]]~~ comprises two-stage etching.

5. (original): The dry etching method according to claim 4, wherein the two-stage etching includes a first stage using a mixed gas of HBr and O₂ and a second stage using a mixed gas of HBr, O₂ and He.

6. (new): The semiconductor device according to claim 1, comprising gate electrodes formed on the N type polysilicon gate and the P type polysilicon gate by polysilicon gate etching.

7. (new): The semiconductor device according to claim 6, wherein the gate electrodes are smaller in area than the N type polysilicon gate or the P type polysilicon gate.

8. (new): The semiconductor device according to claim 1, comprising a plurality of the N type polysilicon gate and the P type polysilicon gate disposed in mixed form.

9. (new): The dry etching method according to claim 3, wherein the step of simultaneously gate-etching the N type polysilicon gate and the P type polysilicon gate comprises polysilicon gate etching to form gate electrodes on the N type polysilicon gate and the P type polysilicon.

10. (new): The dry etching method according to claim 9, wherein the gate electrodes are smaller in area than the N type polysilicon gate or the P type polysilicon gate.

11. (new): The dry etching method according to claim 3, comprising forming a plurality of the N type polysilicon gate and the P type polysilicon gate disposed in mixed form.